ECHO CANCELLATION DEVICE FOR FULL DUPLEX COMMUNICATION SYSTEMS

DESCRIPTION

Cross Reference To Related Applications

[Para 1] This is a continuation-in-part of U.S. Application No. 10/709,935, filed June. 7, 2004, entitled "ECHO CANCELLATION DEVICE FOR A FULL DUPLEX COMMUNICATION SYSTEM", which is cooperated by reference herein.

Background of Invention

[Para 2] 1. Field of the Invention

[Para 3] The present invention relates to a full duplex communication system, and more particularly, to an echo cancellation device for use in a full duplex communication system.

[Para 4] 2. Description of the Prior Art

[Para 5] As technology advances, network applications have become more and more popular. Network bandwidth requirements are also increasing as the transmission speed of data transmission standards such as Ethernet have raised from 10/100Mps to above 1Gbps. As is well known in the art, each port of a 1Gbps fast Ethernet device has four channels, wherein each of the four channels has a transceiver.

[Para 6] Please refer to Fig.1. Fig.1 depicts a simplified schematic diagram of a conventional transceiver 100 in a channel of a 1Gbps Ethernet device. In general, the transceiver 100 is coupled to a twisted pair 118 via a line interface

116. As shown in Fig.1, the transceiver 100 comprises a transmitter section 104 and a receiver section 106. The transmitter section 104 has a digital-to-analog converter (DAC) 108 for converting a transmit signal (a near-end signal) into analog form. The analog transmit signal is then transmitted to a far-end network device via the line interface 116 and the twisted pair 118. The receiver section 106 has an analog-front-end (AFE) circuit 112 for processing a receive signal (a far-end signal) received from the line interface 116, and an analog-to-digital converter (ADC) 114 for converting the processed signals into digital form. The digital signal is then sent to following stages for further processing. The 1Gbps Ethernet device and the far-end network device both simultaneously utilize four channels where each channel simultaneously performs transmitting and receiving operations. As a result, the 1Gbps Ethernet device is a full duplex communication system.

[Para 7] As mentioned above, each channel of the 1Gbps Ethernet device simultaneously performs transmitting and receiving operations. When the channel is transmitting, the signals received from the channel are affected by the transmission, and this phenomenon is known as echo impairment. In order to reduce echo impairment in a communication system, an echo cancellation device 110 and an echo cancellation resistor Rp are usually employed in the conventional transceiver 100. The echo cancellation device 110 is usually a DAC for generating a cancellation signal that corresponds to the transmit signal output from the DAC 108 in order to cancel the effects of the transmit signal on the receiver section 106 and thereby achieve echo cancellation.

[Para 8] Please refer to Fig. 2, which is an equivalent circuit diagram of the conventional transceiver 100 of Fig.1. The electrical equivalence of the DAC 108 and the echo cancellation device 110 are current sources Id and Ic, respectively. In order to achieve echo cancellation for the receiver section 106, the effect caused by the output of the current source Id must be canceled by the output of the current source Ic.

[Para 9] Please refer to FIG. 3, which is a small signal model for the equivalent circuit diagram of Fig.2. In Fig.2, Zo is the equivalent output impedance of the transmitter section 104, and Zi is the equivalent input impedance of the receiver section 106. Vo is the output signal of the transceiver 100 and also the transmit signal output from the transmitter section 104. Vi is the echo on the receiver section 106 caused by the transmit signal. In the conventional art, the echo cancellation device 110 regards the equivalent output impedance Zo as a load resistor Re, and the resistance of the resistor Re consists of a matching resistor Rm, which is used to match impedance, and an equivalent resistor Rc of the channel coupled to the transceiver 100. From the small signal model shown in Fig.3, the following formula can be obtained:

$$Vi = \frac{-Zi\left[IdZo + (Zo + Rp)Ic\right]}{Rp + Zi + Zo}$$

(1)

[Para 10] In order to cancel the echo effect, Vi should be equal to 0, which satisfies:

$$IdZo + (Zo + Rp)Ic = 0$$

(2)

[Para 11] From formula (2), it is known that the relationship between Ic and Id is:

$$Ic = \frac{-Zo}{Rp + Zo} Id$$

(3)

[Para 12] That is to say, if Ic and Id satisfy formula (3), the echo effect will be completely cancelled.

[Para 13] However, as mentioned above, the echo cancellation device 110 regards the equivalent output impedance Zo as the load resistor Re, which consists of the matching resistor Rm and the equivalent resistor Rc of the channel, but ignores an unavoidable parasitic capacitance effect that will occur in a practical implementation. Obviously, the echo effect of the transceiver 100 cannot be effectively reduced to the lowest level if the output impedance Zo is simply viewed as the load resistor Re in the prior art.

[Para 14] Furthermore, from Fig.3, it is known that Vo > Vi. As the working voltage of transceiver ICs becomes lower and lower, both Vo and Vi also become lower and lower. If the working voltage of a transceiver IC becomes lower than a specific level, MOS transistors of the echo cancellation device 110 (electrically equivalent to the current source Ic) may become unable to maintain operation in the saturation region and therefore result in signal distortion in the conventional echo cancellation device 110.

Summary of Invention

[Para 15] It is therefore one of the objectives of the claimed invention to provide an echo cancellation device in a full duplex communication system to solve the parasitical capacitor effect with a filter in order to minimize the echo effect.

[Para 16] Another objective of the claimed invention is maintaining operation in the saturation region for MOS transistors in the echo cancellation device in order to improve the performance of the echo cancellation device.

[Para 17] According to a preferred embodiment of the present invention, an echo cancellation device in a full duplex communication system is disclosed. The full duplex communication system has a transmitter section for transmitting a transmit signal and a receiver section for receiving a receive signal. The echo cancellation device includes a filter for generating a filtering signal according to the transmit signal; an echo canceller coupled to the filter for generating an echo cancellation signal according to the filtering signal; and at least one resistor coupled to the transmitter section, the receiver section, and the echo canceller; wherein the echo canceller further comprises a pull-up current source for increasing the DC level of the echo canceller.

[Para 18] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of Drawings

[Para 19] Fig.1 is a simplified schematic diagram of a conventional transceiver in a channel of a fast Ethernet device.

[Para 20] Fig.2 is an equivalent circuit diagram of the conventional transceiver.

[Para 21] Fig.3 is a small signal model for the equivalent circuit diagram of Fig.2.

[Para 22] Fig.4 is a simplified schematic diagram of a transceiver in a channel of a full duplex communication system according to a first embodiment of the present invention.

[Para 23] Fig.5 and Fig.6 are equivalent circuit diagrams of the transceiver according to the first embodiment of the present invention.

[Para 24] Fig.7 is a simplified schematic diagram of a transceiver in a channel of a full duplex communication system according to a second embodiment of the present invention.

[Para 25] Fig.8 is an equivalent circuit diagram of the transceiver according to the second embodiment of the present invention.

Detailed Description

[Para 26] Please refer to Fig.3. Since the unavoidable parasitic capacitance effect of practical implementations is considered by the present invention, the equivalent output impedance Zo is modified to be the parallel connection of a load resistor Re, which consists of the matching resistor Rm and the equivalent resistor Rc of the channel, and a parasitical capacitor Ce. This means Zo=Re//Ce. The effective output impedance Zo is calculated by the following equation:

$$Zo = \frac{\mathrm{Re}}{s\,\mathrm{Re}\,Ce + 1}$$

(4)

[Para 27] Substitute formula (4) into formula (3) to obtain the following formula (5):

$$Ic = \frac{-\mathrm{Re}}{Rp + \mathrm{Re} + s\,\mathrm{Re}\,RpCe} Id = H(s) \cdot Id$$

(5)

[Para 28] From formula (5), it can be seen that the relationship between Ic and Ic is actually a low pass transfer function H(s).

[Para 29] Please refer to FIG. 4, which depicts a simplified schematic diagram of a transceiver 400 in a channel of a full duplex communication system according to the first embodiment of the present invention. In the transceiver 400, the echo cancellation device of the embodiment of the present invention comprises an echo canceller 410 for generating a cancellation signal corresponding to a transmit signal output from the DAC 408, a resistor Rp coupled between a transmitter section 404 and a receiver section 406 of the transceiver 400, and a low pass filter 420 coupled to the echo canceller 410 as a previous stage of the echo canceller 410. The echo canceller 410 further comprises a pull-up current source for increasing its DC level. In a preferred practical implementation, the echo canceller 410 can be a digital-to-analog converter (DAC).

[Para 30] Fig.5 depicts an equivalent circuit diagram of the transceiver 400 of the embodiment of the present invention. The electrical equivalent of the DAC 408, the echo canceller 410, and the pull-up current source are current sources Id, Ic, and Ia, respectively. The DAC 408 generates a transmit signal according to a digital signal. As mentioned above, the block H(s) shown in Fig.5 is a low pass transfer function and can be implemented to satisfy formula (5) using either a digital means or an analog means. For example, a digital low pass filter can be employed to implement the block H(s). In another embodiment of the present invention, an RC network low pass filter, as shown in Fig.6, can be employed to implement the block H(s). In Fig.6, a capacitor of the RC network low pass filter 420 can be a metal stacked-layer capacitor or a parasitic capacitor, and a resistor of the RC network low pass filter 420 can be a MOS transistor. The resistance of the MOS transistor can be controlled by adjusting its gate voltage Vd.

[Para 31] Since the low pass filter 420 is employed in the echo cancellation device of the embodiment of the present invention, the cancellation signal output from the echo canceller 410 is capable of canceling the echo effect

caused by the transmit signal output from the DAC 408, which is electrical equivalence as the current source Id. Wherein, the echo canceller 410 is the electrical equivalent of the current source Ic. The echo effect on the receiver section 406 is thereby minimized.

[Para 32] In addition, the echo cancellation device of the embodiment of the present invention further utilizes the pull-up current source, which is the electrical equivalent of the current source Ia in Fig.5 and Fig.6, to increase the DC level of Vi. Therefore, the MOS transistors of the equivalent current source Ic can maintain operation in the saturation region to avoid signal distortion. The echo cancellation performance of the echo canceller 410 of the present invention is thereby improved. In practical implementations, the pull-up current source (the equivalent current source Ia) can be a fix current source or an adjustable current source. That is to say, the output of the equivalent current source Ia can be a DC or an AC signal with a fixed DC level, or a DC or an AC signal with a DC level changing with the magnitude of the current source Ic.

[Para 33] Fig.7 depicts a simplified schematic diagram of a transceiver 700 in a channel of a full duplex communication system according to a second embodiment of the present invention. In practical implementations, the capacitance of the parasitic capacitor Ce, the resistance of the channel's equivalent resistor Rc, and the impedance of the matching resistor Rm is affected by the operating environment, temperature, manufacturing deviations, or the similar variations. Therefore the values will fluctuate and change when transmitting/receiving data. In order to more precisely eliminate the echo, in the second embodiment of the present invention, the echo cancellation device further comprises an echo residue detector 722 for detecting the echo residue at the receiver section 706. The echo residue detector 722 generates a control signal according to the detected echo residue and outputs the control signal to a low pass filter 720 to adjust the poles of the low pass transfer function H(s) to minimize the echo residue.

[Para 34] Please refer to Fig.8, which depicts an equivalent circuit diagram of the transceiver 700 of the present invention. In Fig.8, if the low pass filter 720 is a digital low pass filter, the echo residue detector 722 dynamically adjusts the finite impulse response (FIR) coefficients or the infinite impulse response (IIR) coefficients of the digital low pass filter according to the detected echo residue. If the low pass filter 720 is an RC network low pass filter, the echo residue detector 722 dynamically adjusts the gate voltage Vd to change the RC value of the RC network low pass filter 720 according to the detected echo residue. Thus, the echo cancellation device of the present invention obtains optimal performance by dynamically adjusting the low pass filter 720 according to the different characteristics of circuit components and the network environment. The function and implementation means of the pull-up current source Ia in Fig.8 is substantially the same as the pull-up current source Ia in Fig.4, therefore, further details are omitted here for brevity.

[Para 35] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.